Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (currently amended) An electrostatic discharge protection circuit for an input/output signal terminal in an integrated circuit, coupled to ground comprising:

~~an input;~~

a diode string coupled to the input/output signal terminal;

a transistor switch having its gate coupled to the diode string, the transistor switch coupling the input/output signal terminal to ground in parallel to the diode string;

~~and~~

a reverse diode coupling ground to the input/output signal terminal; and

a capacitive element in series with the transistor switch to reduce the capacitance contributed by the transistor switch, thereby reducing signal distortion

whereby voltage overload protection for RF power amplifiers is provided for the conditions of (1) output impedance mismatch, (2) RF overdrive, and (3) modulated input signal.

2. - 4. (cancelled)

5. (currently amended) The electrostatic discharge protection circuit of claim 1 ~~4~~ where the ~~switching~~ transistor switch comprises a Darlington pair and the capacitive element comprises a diode.

6. (currently amended) The electrostatic discharge protection circuit of claim 1 where the transistor switch comprises a Darlington pair and further comprising a series diode and a series resistor combined in any order and coupled between the gate of the transistor switch and the diode string on one hand and ground on the other hand.

7. (cancelled)

8. (original) The electrostatic discharge protection circuit of claim 1 where the diode string, transistor switch and reverse diode is fabricated in GaAs, InP, SiGe, or other compound semiconductor.

9. (currently amended) The electrostatic discharge protection circuit of claim 1 where the electrostatic discharge protection circuit is integrally coupled to the input/output signal terminal of an RF integrated circuit.

10. (cancelled)

11. (currently amended) An integrated electrostatic discharge protection circuit for an input/output signal terminal in an integrated RF circuit ~~coupled to ground~~ comprising:

~~an input;~~

a diode string coupled to the input/output signal terminal;

a Darlington pair having its gate coupled to the diode string, the Darlington pair coupling the input/output signal terminal to ground in parallel to the diode string;

a series diode;

a series resistor, where the series diode and the series resistor are coupled in series with each other to reduce the leakage current at low and medium RF power operation and their combination is coupled between the gate of the Darlington pair and diode string on one hand and ground on the other hand;

a diode in series with the Darlington pair to reduce the capacitance contributed by the Darlington pair, thereby reducing signal distortion; and

a reverse diode coupling ground to the input/output signal terminal where the diode string is forward biased on the application of positive ESD events at the input and the reverse diode is forward biased on the application of negative ESD events at the input,

whereby voltage overload protection for RF power amplifiers is provided for the conditions of (1) output impedance mismatch, (2) RF overdrive, and (3) modulated input signal.

12. (currently amended) A method for providing electrostatic discharge protection for an input/output signal terminal of an integrated circuit comprising:

sinking a first type of ESD event to ground from the input/output signal terminal ~~an input~~ through a diode string coupled to the input/output signal terminal by triggering a transistor switch having its gate coupled to the diode string, the transistor switch coupling the input/output signal terminal to ground in parallel to the diode string; ~~and~~

sinking a second type of ESD event through a reverse diode coupling ground to the input/output signal terminal; and

coupling the input/output signal terminal to ground during ESD protection by means of a capacitive element in series with the transistor switch to reduce the capacitance contributed from the transistor switch ,thereby reducing signal distortion.

13. (original) The method of claim 12 where the first type of ESD event is a positive voltage surge applied to the input, and the second type of ESD event is a negative voltage surge applied to the input.

14. (original) The method of claim 12 where triggering the transistor switch comprises triggering a Darlington pair.

15. (original) The method of claim 14 where triggering the Darlington pair comprises coupling the first type of ESD event through the diode string to the gate of the Darlington pair while also coupling the first type of ESD event through the diode string to a series diode and resistor to ground to prevent the ESD protection circuit from turning on during low to moderate RF power operation, therefore minimizing leaking current and improving linearity.

16. (cancelled)

17. (currently amended) The method of claim 12 ~~16~~ where coupling the input to ground during ESD protection comprises coupling the input to ground by means of a diode in series with a Darlington pair to reduce the capacitance contributed from the Darlington pair, thereby reducing signal distortion.

18. (currently amended) A method for providing electrostatic discharge protection comprising:

sinking a first type of ESD event to ground from an input through a diode string coupled to the input/output signal terminal by triggering a Darlington pair having its gate coupled to the diode string, the Darlington pair coupling the input to ground in parallel to the diode string, where coupling the first type of ESD event through the diode string to the gate of the Darlington pair also couples the first type of ESD event through the diode string to a series diode and resistor to ground to prevent the ESD protection circuit from turning on during low to moderate RF power operation, therefore minimizing leaking current and improving linearity, while also coupling the input/output signal terminal to ground during the ESD protection by means of a diode in series with the Darlington pair to reduce the capacitance contributed to the diode string from the Darlington pair, thereby reducing signal distortion; and

sinking a second type of ESD event through a reverse diode coupling ground to the input/output signal terminal; and

coupling the input/output signal terminal to ground during ESD protection by means of a capacitive element in series with the transistor switch to reduce the capacitance contributed from the transistor switch, thereby reducing signal distortion.

19. (original) The method of claim 18 where the first type of ESD event is a positive voltage surge applied to the input, and the second type of ESD event is a negative voltage surge applied to the input.

20. (original) The method of claim 18 where the first type of ESD event is a negative voltage surge applied to the input, and the second type of ESD event is a positive voltage surge applied to the input.

21. (original) The circuit of claim 1 where the diode string is comprised of a plurality of BC junction diodes.

22. (original) The circuit of claim 1 where the diode string is comprised of a plurality of BE junction diodes.

23. (original) The circuit of claim 1 where the diode string is comprised of a plurality of isolated implanted base emitter diodes in SiGe HBT technology, or a plurality of epi base emitter or base collector diodes in compound semiconductor technology, including GaAs, InP or other compound semiconductor.

24. (cancelled)

25. (currently amended) An ESD protected bonding pad comprising:

a first pad;

a diode string coupled to the first pad;

a transistor switch having its gate coupled to the diode string, the transistor switch coupling the first pad to ground in parallel to the diode string; ~~and~~

a reverse diode coupling ground to the first pad; and

a capacitive element in series with the transistor switch to reduce the capacitance contributed by the transistor switch, thereby reducing signal distortion.

26. (currently amended) An ESD protected integrated circuit input comprising:

an integrated circuit input;

a diode string coupled to the integrated circuit input;

a transistor switch having its gate coupled to the diode string, the transistor switch coupling the integrated circuit input to ground in parallel to the diode string; ~~and~~

a reverse diode coupling ground to the integrated circuit input; and

a capacitive element in series with the transistor switch to reduce the capacitance contributed by the transistor switch, thereby reducing signal distortion.

27. (original) The electrostatic discharge protection circuit of claim 1 wherein the transistor switch and diode string each have a chip-layout size and where the chip-layout size of the transistor switch and diode string when used in combination is smaller

than the chip-layout size of a diode string when used alone, which used-alone diode string provides substantially the same ESD protection as the transistor switch and diode string in combination as characterized by the maximum clamping voltage of the electrostatic discharge protection circuit.

28. – 29. (cancelled)

30. (original) The electrostatic discharge protection circuit of claim 27 wherein the electrostatic discharge protection circuit is disposed in unused space on a chip between adjacent bonding pads.